Abstract

A device (1) to control processing of data elements (data_i), in which a thread is assigned to each data element (data_i), comprises a first unit (CS), which, during a first cycle, fetches an instruction (cs_ir_s) that is entered in the context of the thread assigned to the incoming data element (data_i), a second unit (IF), which, during a second cycle, fetches an instruction (if_ir_s) that succeeds a stipulated instruction in a stipulated thread, and a third unit (ID), which, during the second cycle, decodes the instruction prescribed for processing of the data element (data_i) and generates a data element processing signal (dec_o).